Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-15 (Canceled)

Claim 16 (Previously presented): A semiconductor wafer comprising:

a plurality of dies each comprising functional circuitry;

electrically conductive structures configured to contactlessly receive test signals for testing said functional circuitry; and

an electrically conductive shielding plane disposed between ones of said conductive structures and said functional circuitry of at least one of said dies.

Claim 17 (Original): The semiconductor wafer of claim 16, wherein each die comprises a set of said conductive structures.

Claim 18 (Original): The semiconductor wafer of claim 16, wherein each of said conductive structures in a set of said conductive structures are electrically connected to a plurality of said dies.

Claim 19 (Original): The semiconductor wafer of claim 16, wherein said conductive structures are electromagnetically coupleable to a tester interface device.

Claim 20 (Original): The semiconductor wafer of claim 16 further comprising a transmitter configured to transmit test signals on at least one of said conductive structures.

Claim 21 (Original): The semiconductor wafer of claim 20, wherein each of said dies comprises such a transmitter.

Claim 22 (Original): The semiconductor wafer of claim 16 further comprising a receiver configured to receive a test signal induced on at least one of said conductive structures.

Claim 23 (Original): The semiconductor wafer of claim 22, wherein each of said dies comprises such a receiver.

Claim 24 (Original): The semiconductor wafer of claim 16 further comprising a transceiver configured to transmit test signals on at least one of said conductive structures and to receive a test signal induced on at least one of said conductive structures.

Claim 25 (Original): The semiconductor wafer of claim 24, wherein each of said dies comprises such a transceiver.

Claim 26 (Original): The semiconductor wafer of claim 16 further comprising built in self test circuitry.

Claim 27 (Previously presented): A semiconductor wafer comprising:

a plurality of dies each comprising functional circuitry;

means for receiving a test signal from a tester channel without physically contacting said tester channel; and

an electrically conductive shielding plane disposed between said means for receiving a test signal and said functional circuitry of at least one of said dies.

Claim 28 (Original): The semiconductor wafer of claim 27 further comprising means for sending a test signal to a test channel without physically contacting said tester channel.

Claim 29 (Original): The semiconductor wafer of claim 27, wherein said means for receiving receives a plurality of test signals from a plurality of tester channels without physically contacting said plurality of tester channels.

Claim 30 (Original): The semiconductor wafer of claim 27 further comprising means for controlling communications with a plurality of said tester channels.

Claims 31-35 (Canceled)

Claim 36 (Previously presented): The semiconductor wafer of claim 27, wherein:

each die further comprises communications control circuitry; and

ones of said means for receiving a test signal are electrically connected to said communications control circuitry through openings in said plane.

Claim 37 (Previously presented): The semiconductor wafer of claim 36, wherein at least one of said means for receiving a test signal is electrically connected to said communications control circuitry and to said plane.

Claim 38 (Previously presented): The semiconductor wafer of claim 37, wherein said plane is a ground plane.

Claim 39 (Currently amended): The semiconductor wafer of claim 16 further comprising:

a plurality of electrically conductive planes disposed between said conductive structures and said functional circuitry; and

insulating material disposed between said planes.

Claim 40 (Previously presented): The semiconductor wafer of claim 39, wherein one of said planes is configured as a power distribution plane, and another of said planes is configured as a ground plane.

Claim 41 (Currently amended): The semiconductor wafer of claim 16, wherein:

each die further comprises communications control circuitry; and

ones of said conductive structures are electrically connected to said communications control circuitry through openings in said plane.

Claim 42 (Previously presented): The semiconductor wafer of claim 41, wherein at least one of said conductive structures is electrically connected at one end to said communications control circuitry and is electrically connected at another end to said plane.

Claim 43 (Previously presented): The semiconductor wafer of claim 42, wherein said plane is a ground plane.

Claim 44 (Currently amended): The semiconductor wafer of claim [[16]] 27 further comprising:

a plurality of electrically conductive planes disposed between said conductive structures and said functional circuitry; and

insulating material disposed between said planes.

Claim 45 (Previously presented): The semiconductor wafer of claim 44, wherein one of said planes is configured as a power distribution plane, and another of said planes is configured as a ground plane.

Claim 46 (Previously presented): The semiconductor wafer of 16, wherein said electrically conductive shielding plane is a shield structure disposed to shield at least one of said dies from electrical interference.

Claim 47 (Previously presented): The semiconductor wafer of 16, wherein said electrically conductive shielding plane is sized to substantially cover at least one of said dies.

Claim 48 (Previously presented): The semiconductor wafer of 27, wherein said electrically conductive shielding plane is a shield structure disposed to shield at least one of said dies from electrical interference.

Claim 49 (Previously presented): The semiconductor wafer of 27, wherein said electrically conductive shielding plane is sized to substantially cover at least one of said dies.

Claim 50 (New): The semiconductor wafer of 16, wherein said shielding plane comprises openings through which said conductive structures are electrically connected to said functional circuitry of said at least one of said dies.

Claim 51 (New): The semiconductor wafer of claim 47, wherein said shielding plane is a solid plate structure.

Claim 52 (New): The semiconductor wafer of 27, wherein said shielding plane comprises openings through which said means for receiving a test signal is electrically connected to said functional circuitry of said at least one of said dies.

Claim 53 (New): The semiconductor wafer of claim 49, wherein said shielding plane is a solid plate structure.